Application No. 09/160,157
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This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-39 (cancelled)

Claim 40. (previously presented) A semiconductor device comprising an n-channel field effect transistor including a drain formed in a semiconductive layer, a source formed in said semiconductive layer, a channel extending between the drain and the source, a gate insulating layer over said channel, an interface between a semiconductive silicon layer and a gate insulating layer, and conductive contacts to said drain, source and on said gate insulating layer, said field effect transistor structurally characterized by the retention of deuterium at said interface resulting from post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature above about 200°C so as to increase the resilience of the field effect transistor to hot electron effects during operation.

Claim 41. (previously presented) The semiconductor device of claim 40 wherein said gate insulating layer comprises silicon dioxide.

Claims 42-46 (cancelled)

Claim 47. (previously presented) The semiconductor device of claim 40, which is encapsulated.

Claims 48 -59 (cancelled)

Claim 60. (previously presented) The semiconductor device of claim 40, wherein said gate insulating layer comprises an oxide of silicon.

Claim 61. (previously presented) The semiconductor device of claim 40, wherein said gate insulating layer comprises silicon dioxide or silicon oxy nitride.

Claim 62. (previously presented) A semiconductor device comprising an n-channel field effect transistor having an interface between a semiconductive silicon layer and a gate insulating layer having a thickness not exceeding about 55 Angstroms, a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate insulating layer over said channel, said interface between said gate insulating layer and said channel, and conductive contacts for said drain, said source and said gate insulating layer; said semiconductive device structurally characterized by post-fabrication heating of the device after formation of at least said gate contact, in a deuterium gas-enriched atmosphere at a temperature above about 200°C to provide deuterium at and to passivate said interface so as to increase the resilience of the field effect transistor to hot electron effects.

Claim 63. (previously presented) The semiconductor device of claim 62 wherein said gate insulating layer comprises silicon oxide.

Claim 64. (previously presented) The semiconductor device of claim 62, wherein said gate insulating comprises silicon oxynitride.

Claim 65. (previously presented) The semiconductor device of claim 62, comprising deuterium atoms from said post-fabrication passivation covalently bonded at said interface.

Claims 66 - 75 (Cancelled)

Claim 76. (previously presented) A semiconductor device comprising a field effect transistor having a gate dielectric film having a thickness not exceeding about 55 Angstroms disposed between a transistor gate contact and a semiconductive layer that includes doped source and drain regions and contacts to said doped source and drain regions, said semiconductor device structurally characterized by a concentration of deuterium in said gate dielectric film at an interface with said semiconductive layer provided by heating the device,

after formation of said source, drain and gate contacts, at a temperature of about 400°C for about one hour in an atmosphere comprising about 10% deuterium and about 90% nitrogen, said transistor device susceptible to degradation associated with hot carrier stress, and said concentration of deuterium increasing the resilience of the field effect transistor to channel hot carrier stress.

Claim 77. (previously presented) A semiconductor device according to claim 76 wherein the semiconductive layer comprises silicon, and the gate dielectric film includes a silicon compound.

Claim 78. (previously presented) A semiconductor device according to claim 77 wherein said silicon compound comprises an oxygen or a nitrogen containing silicon compound.

Claim 79. (previously presented) A semiconductor device comprising a field effect transistor having an interface between a semiconductive silicon layer and a gate insulating layer, structurally characterized by the gate insulating layer having a thickness not exceeding about 55 Angstroms and by the presence of deuterium at said interface resulting from post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature above about 200°C so as to increase the resilience of the field effect transistor to hot electron effects, said post-fabrication passivation being conducted sufficiently to provide to said transistor a practical lifetime at least about ten times that provided by a corresponding passivation with hydrogen, wherein practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.

Claim 80. (previously presented) A semiconductor device comprising an NMOS field effect transistor having an interface between a semiconductive silicon layer and a gate insulating layer, a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate insulating layer over said channel, said interface between said gate insulating layer and said channel, and conductive contacts for said drain, said source and said gate insulating layer; said semiconductive device structurally characterized by said gate insulating layer having a thickness

not exceeding about 55 Angstroms and by annealing of the device after formation of at least said gate contact, in a deuterium gas-enriched atmosphere at a temperature above about 200°C to provide deuterium at said interface between said gate insulating layer and said channel to passivate said interface so as to increase the resilience of the field effect transistor to hot electron effects.

Claim 81. (currently amended) An improved semiconductor device including an insulated gate field effect transistor device having a transistor gate and a gate insulator film not exceeding about 55 Angstroms thickness interposed between said transistor gate and a channel of said transistor device, said transistor device including source, drain and gate contacts, and a concentration of deuterium introduced into and remaining ~~within~~ said interposed gate insulator film, said transistor device susceptible to degradation associated with hot carrier stress, said concentration of deuterium substantially reducing said degradation associated with said hot carrier stress.

Claim 82. (previously presented) An improved semiconductor device according to claim 81, wherein said gate insulator comprises an oxide of silicon.

Claim 83. (previously presented) An improved semiconductor device according to claim 81, wherein said gate insulator comprises silicon oxynitride.

Claim 84. (previously presented) An improved semiconductor device according to claim 81, wherein the field effect transistor comprises an n-channel device subject in operation to hot electron stress.